Remarks

Applicant is providing amended drawings with functional descriptions, as requested in the Office action.

The specification has been amended to make a correction to paragraph [41], which is paragraph [87] of the application as published under Pub. No. 2004/0199674, to require a *galvanic* decoupling device. The relevant sentence therefore properly reads

> "Here, the communication is realized over a **galvanic** decoupling device 2, which can be, e.g., an optocoupler, a magnetocoupler, a transformer, or some other known device for decoupling."

The corresponding sentence is in the largest paragraph on page 11 of the German priority document, which reads

> "Die Kommunikation erfolgt hier über eine **galvanische** Trennung 2, die biespielweise ein Oktokoppler ...."

The present application states in paragraph [18], which is paragraph [25] of Pub. 2004/0199674, that the entire disclosure of the German priority document is explicitly incorporated by reference. This correction is therefore proper.

Reconsideration is respectfully requested of the rejection of pending claims 1, 3, 5-11, and 13-19 under 35 USC 112. Applicant has amended claims 1, 3, 14, and 15 to recite the essential cooperative relationships of the elements, and the relationship of each element to the system has been inserted. Applicant has cancelled claims 2, 4, and 12.

Reconsideration is respectfully requested of the rejection of claims 1, 3, 5-11, and 13-19 under 35 USC 102 in view of Schlotterer et al. 5,751,234.

Schlotterer et al. disclose a hybrid monolithic IC that is standardized for controlling various types of electrical equipment. Schlotterer et al. use one single IC which includes an on-board

microprocessor, an analog-to-digital-subsystem, and various input/output devices on a single monolitic chip. The IC also includes an analog subsystem identified by function blocks 62 and 64 in Fig. 2. The general goal of Schlotterer is to integrate a complete control circuit for several inputs into one single IC.

Schlotterer et al. employ a relatively complex system of a CPU within the IC. The circuit itself is conventional: it uses multiplexers to achieve an auto ranging circuit for different voltage and current levels. For this purpose an analog/digital converter is used in order to read the result by the CPU and to prepare the multiplexers for the auto ranging. Schlotterer et al. use components including switches and multiplexers, but for a completely different purpose than defined in the present claims.

In contrast to the Schlotterer et al. system, the present invention is directed to an IC by which it is possible to configure an I/O-pin in such a way that it can perform different functions. For example: a) simple functions such as analog and digital input or output, or b) complex functions like counters and control circuits. In accordance with the invention, the individual functions required are separated into subfunctions. One part is performed by the front-end circuit (interface circuit chip 1), whereas the other part is located in the logic circuit (3). Circuits 1 and 3 communicate with each other *only* via two digital lines (IN and OUT) making the galvanic decoupling very simple, for example by using only two optocouplers.

Turning now to claim 1, Schlotterer does not disclose or suggest the express requirement that an interface circuit chip and a logic circuit are connected with each other by a galvanic coupling device. Rather, in the Schlotterer patent, a single IC is used to control various types of electrical equipment:

> Briefly, the present invention relates to a monolithic IC that is standardized for controlling various types of electrical equipment, such as circuit breakers, motor controllers and the like. The IC is a monolithic IC, fabricated in CMOS technology. The shortcomings of utilizing CMOS technology for linear or analog circuitry is overcome by the implementation of the IC to provide a monolithic IC that is relatively less expensive than using multiple ICs or a single IC fabricated from biCMOS technology. Column 2, lines 29-57.

Particularly, Schlotterer et al.'s single IC includes "an on-board microprocessor, an A/D subsystem and various input/output devices ...." Col. 2, lines 60-62. All subsystems on the single IC communicate with each other via lines:

> The microprocessor 30 communicates with the various other peripherals and external pins on the chip 10 by way of an internal address, data and control bus 34. Col. 6, lines 18-20.

Thus, Schlotterer et al. fail to teach or suggest any galvanic decoupling device.

Furthermore, Schlotterer et al. do not disclose or suggest the express requirement of both an analog comparator and a digital/analog converter whose inputs are connected to outputs of a multiplexer, whose input is connected to output of a switch, whose input is connected to a bidirectional input connection which is connected to a logic circuit. Rather, in the Schlotterer patent, only an analog/digital converter is disclosed.[1] Accordingly, the analog subsystem disclosed by Schlotterer et al. merely includes analog input channels for receiving analog voltage and current signals and converting these signals to a digital signal:

---

[1] Schlotterer, Fig. 3, reference numeral 78.

> An important aspect of the invention relates to an analog subsystem, identified by the function blocks 62 and 64 in FIG. 2. A block diagram for this subsystem is illustrated in FIG. 3. The analog subsystem includes, for example, six analog input channels for receiving analog voltage and current signals and converting these signals to an 8-bit digital signal with 12-bit resolution. Four of the input channels 62 can be selected by the software to operate as either voltage inputs or current inputs. The other input channels 64 can only be operated as voltage inputs.

Thus, Schlotterer et al. merely provide a digital output signal:

> There are other important aspects of the invention. For example, the IC 10 is adapted to respond to either analog signals or digital signals and provide a digital output signal. Col. 8, lines 61-63.

And there is no suggestion to provide both digital and analog output signals, responsive to the input signals.

And claim 1 is further patentable because Schlotterer et al. do not disclose or suggest the requirement that the switches, multiplexers, analog comparators, and digital/analog converters are activated, deactivated, or changeable with different analog or digital functions being assignable to the one or more bidirectional input connections. Rather, in the Schlotterer et al. patent, each of the IC pins is defined as either an analog pin or a digital pin. Thus, Schlotterer et al. merely disclose bidirectional input connections having digital functions.[2] Moreover, as discussed above, the Schlotterer et al. IC only provides a digital output from a particular digital or analog input signal.[3] Thus, the Schlotterer IC can only assign digital functions to the input connections rather

---

[2] Schlotterer et al., col. 64 line 20 – col. 66.

[3] Schlotterer et al., col. 8, lines 61-63. (quoted above)

than both digital and analog functions.[4] As a result, Schlotterer et al. fail to disclose many advantages provided by the present invention. For example, because "the physical properties of each I/O pin are programmable, with each I/O pin being able to assume a wide range of functions as digital or analog inputs or outputs" the present invention provides "a universal interface circuit."[5]

In view of the foregoing, claim 1 and claims 3, 5-11, and 13-19 dependent therefrom are respectfully submitted to be patentable over the cited art.

[4] Schlotterer, col. 64 line 20 – col. 66.

[5] Application, paragraph [19]; see also paragraph [12].

CONCLUSION

Applicant requests the entry of this Amendment and issuance of a Notice of Allowance for claims 1, 3, 5-11, and 13-19.

The Commissioner is hereby authorized to charge the fee for the three-month extension of time in the amount of $510 to Deposit Account No. 19-1345. The Commissioner is hereby authorized to charge any additional fees which may be required to Deposit Account No. 19-1345.

Respectfully submitted,

/paul fleischut/

Paul I. J. Fleischut, Reg. No. 35,513
SENNIGER POWERS
One Metropolitan Square, 16th Floor
St. Louis, Missouri 63102
(314) 231-5400

PIF/leb
*Enclosure (Amended Drawings)

Filed via EFS